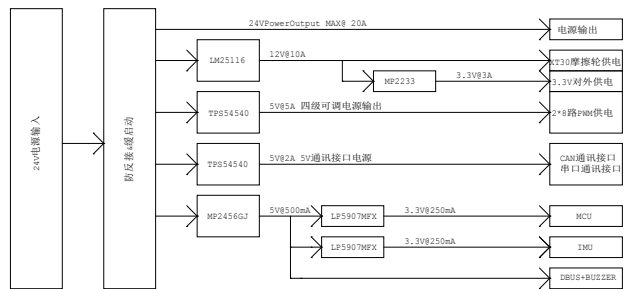
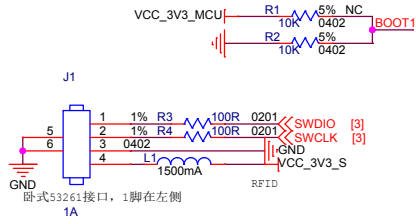


PowerTree

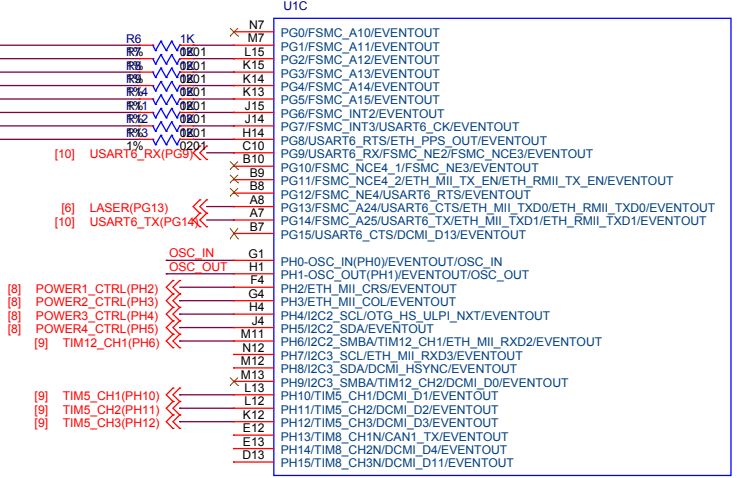
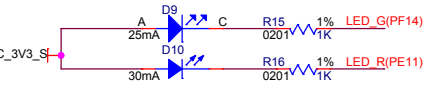
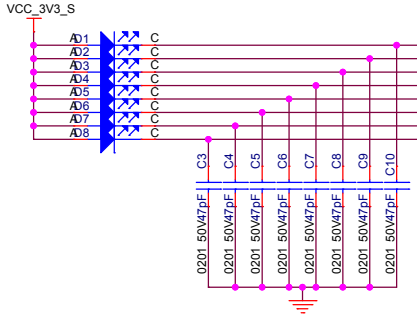
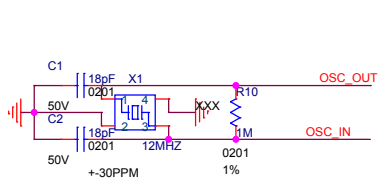




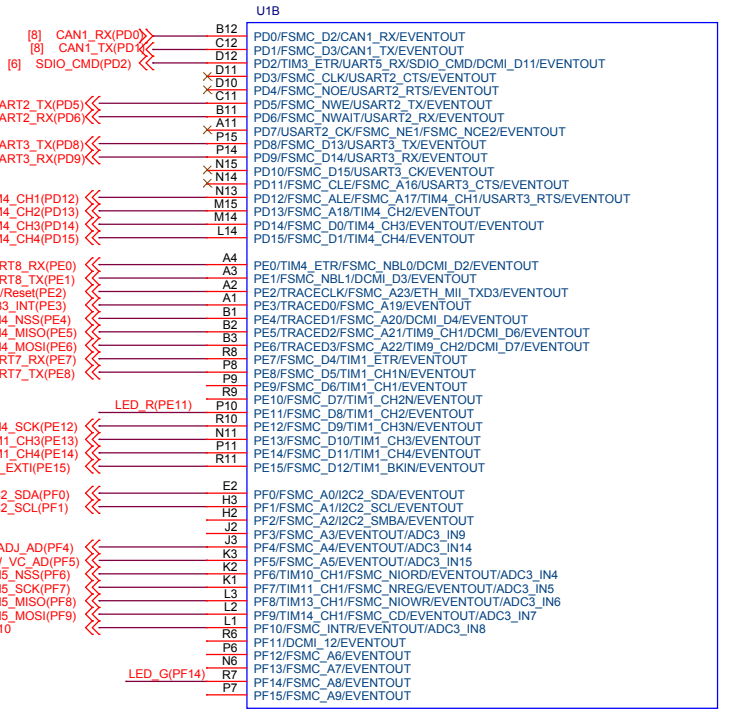
U1A	
[9]	TIM2_CH1(PA0) << N3
[9]	TIM2_CH2(PA1) << N2
[9]	TIM2_CH3(PA2) << P2
[9]	TIM2_CH4(PA3) << N4
[9]	DAC_OUT1(PA4) << P4
[9]	DAC_OUT2(PA5) << P3
[6]	BUTTON_AD(PA6) << R3
[6]	OLED_MOSI(PA7) << F15
[9]	TIM1_CH1(PA8) << E15
[9]	TIM1_CH2(PA9) << D15
[6]	USB_FS_ID(PA10) << C15
[6]	USB_FS_DM(PA11) << B15
[6]	USB_FS_DP(PA12) << A15
[3]	SWDIO << A14
[3]	SWCLK << A13
[9]	ADC1_IN8(PB0) << R5
[9]	ADC1_IN9(PB1) << R4
[9]	KEY(PB2) << BOOT1 M6
[6]	OLED_SCLK(PB3) << A10
[7]	Heat_PWM(PB5) << A9
[9]	USART1_RX(PB7) << A6
[7]	IMU_INT(PB8) << B5
[6]	OLED_DC(PB9) << A5
[6]	OLED_RST(PB10) << B4
[8]	CAN2_RX(PB12) << R12
[8]	CAN2_TX(PB13) << R13
[10]	SNYCHOR(PB14) << P12
[10]	SNYCHOR(PB15) << P13
[9]	ADC1_IN10(PC0) << R15
[9]	ADC1_IN11(PC1) << M2
[9]	ADC1_IN12(PC2) << M3
[9]	ADC1_IN13(PC3) << M4
[9]	ADC1_IN14(PC4) << M5
[9]	ADC1_IN15(PC5) << N5
[6]	SDIO_D0(PC8) << P5
[6]	SDIO_D1(PC9) << H15
[6]	SDIO_D2(PC10) << G15
[6]	SDIO_D3(PC11) << G14
[6]	SDIO_CK(PC12) << F14
	<< B14
	<< B13
	<< A12
	<< D1
	<< E1
	<< F1
	PA0_WKUP/USART2_CTS/UART4_TX/ETH_MII CRS/TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR/EVENTOUT/ADC123_IN0/WKUP
	PA1/USART2_RTS/UART4_RX/ETH_RMII_REF_CLK/ETH_MII_RX_CLK/TIM5_CH2/TIM2_CH2/EVENTOUT/ADC123_IN2
	PA2/USART2_TX/TIM5_CH3/TIM9_CH1/TIM2_CH3/ETH_MDIO/EVENTOUT/ADC123_IN2
	PA3/USART2_RX/TIM5_CH4/TIM9_CH2/TIM2_CH4/OTG_HS_ULPI_D0/ETH_MII_COL/EVENTOUT/ADC123_IN3
	PA4/SP1_NSS/SP3_NSS/USART2_CK/DCMI_HSYNC/OTG_HS_SOF/I2S3_WS/EVENTOUT/ADC12_IN4/DAC_OUT1
	PA5/SP1_SCK/OTG_HS_ULPI_CK/TIM2_CH1_ETR/TIM8_CH1/EVENTOUT/ADC12_IN5/DAC2_OUT
	PA6/SP1_MISO/TIM8_BKIN/TIM13_CH1/DCMI_PIXCLK/TIM3_CH1/TIM1_BKIN/EVENTOUT/ADC12_IN6
	PA7/SP1_MOSI/TIM8_CH1/TIM14_CH1/TIM3_CH2/ETH_MII_RX_DV/TIM1_CH1/RMII_CRS_DV/EVENTOUT/ADC12_IN7
	PA8/MCO1/USART1_CK/TIM1_CH1/I2C3_SCL/OTG_FS_SOF/EVENTOUT
	PA9/USART1_TX/TIM1_CH2/I2C3_SMBA/DCMI_D0/EVENTOUT/OTG_FS_VBUS
	PA10/USART1_RX/TIM1_CH3/OTG_FS_ID/DCMI_D1/EVENTOUT
	PA11/USART1_CTS/CAN1_RX/TIM1_CH4/OTG_FS_DM/EVENTOUT
	PA12/USART1_RTS/CAN1_TX/TIM1_ETR/OTG_FS_DP/EVENTOUT
	PA13/JTMS-SWDIO/JTMS-SWDIO/EVENTOUT
	PA14/JTCK-SWCLK/JTCK-SWCLK/EVENTOUT
	PA15/JTDI/JTDI/SP3_NSS/I2S3_WS/TIM2_CH1_ETR/SP1_NSS/EVENTOUT
	PB0/TIM3_CH3/TIM8_CH2N/OTG_HS_ULPI_D1/ETH_MII_RXD2/TIM1_CH2N/EVENTOUT/ADC12_IN8
	PB1/TIM3_CH4/TIM8_CH3N/OTG_HS_ULPI_D2/ETH_MII_RXD3/OTG_HS_INTN/TIM1_CH3N/EVENTOUT/ADC12_IN9
	PB2/PB2_BOOT1/EVENTOUT
	PB3/JTDO/TRACESWO/JTDO/TRACESWO/SP3_SCK/I2S3_CK/TIM2_CH2/SP1_SCK/EVENTOUT
	PB4/NJTRST/NJTRST/SP3_MISO/TIM3_CH1/SP1_MISO/I2S3ext_SD/EVENTOUT
	PB5/I2C1_SMBA/CAN2_RX/OTG_HS_ULPI_D7/ETH_PPS_OUT/TIM3_CH2/SP1_MOSI/DCMI_D10/I2S3_SD/EVENTOUT
	PB6/I2C1_SCL/TIM4_CH1/CAN2_TX/DCMI_D5/USART1_TX/EVENTOUT
	PB7/I2C1_SDA/FSMC_NL/DCMI_VSYNC/USART1_RX/TIM4_CH2/EVENTOUT
	PB8/TIM4_CH3/SDIO_D4/TIM10_CH1/DCMI_D6/ETH_MII_TXD3/I2C1_SCL/CAN1_RX/EVENTOUT
	PB9/SP2_NSS/I2S2_WS/TIM4_CH4/TIM11_CH1/SDIO_D5/DCMI_D7/I2C1_SDA/CAN1_TX/EVENTOUT
	PB10/SP2_SCK/I2S2_CK/I2C2_SCL/USART3_TX/OTG_HS_ULPI_D3/ETH_MII_RX_ER/TIM2_CH3/EVENTOUT
	PB11/I2C2_SDA/USART3_RX/OTG_HS_ULPI_D4/ETH_RMII_TX_EN/ETH_MII_TX_EN/TIM2_CH4/EVENTOUT
	PB12/SP2_NSSI/I2S2_WS/I2C2_SMBA/USART3_CK/TIM1_BKIN/CAN2_RX/OTG_HS_ULPI_D5/ETH_RMII_TXD0/ETH_MII_TXD0/OTG_HS_ID/EVENTOUT
	PB13/SP2_SCK/I2S2_CK/USART3_CTS/TIM1_CH1N/CAN2_TX/OTG_HS_ULPI_D6/ETH_RMII_TXD1/ETH_MII_TXD1/EVENTOUT/OTG_HS_VBUS
	PB14/SP2_MISO/TIM1_CH2N/TIM2_CH1/OTG_HS_DM/USART3_RTS/TIM8_CH2N/I2S2ext_SD/EVENTOUT
	PB15/SP2_MOSI/I2S2_SD/TIM1_CH3N/TIM8_CH3N/TIM12_CH2/OTG_HS_DP/EVENTOUT
	PC0/OTG_HS_ULPI_STP/EVENTOUT/ADC123_IN10
	PC1/ETH_MDCC/EVENTOUT/ADC123_IN11
	PC2/SP2_MISO/OTG_HS_ULPI_DIR/TH_MII_TXD2/I2S2ext_SD/EVENTOUT/ADC123_IN12
	PC3/SP2_MOSI/I2S2_SD/OTG_HS_ULPI_NXT/ETH_MII_TX_CLK/EVENTOUT/ADC123_IN13
	PC4/ETH_RMII_RX_D0/ETH_MII_RX_D0/EVENTOUT/ADC12_IN14
	PC5/ETH_RMII_RX_D1/ETH_MII_RX_D1/EVENTOUT/ADC12_IN15
	PC6/I2S2_MCK/TIM8_CH1/SDIO_D6/USART6_TX/DCMI_D0/TIM3_CH1/EVENTOUT
	PC7/I2S3_MCK/TIM8_CH2/SDIO_D7/USART6_RX/DCMI_D1/TIM3_CH2/EVENTOUT
	PC8/TIM8_CH3/SDIO_D0/TIM3_CH3/USART6_CK/DCMI_D2/EVENTOUT
	PC9/I2S_CKIN/MCO2/TIM8_CH4/SDIO_D1/I2C3_SDA/DCMI_D3/TIM3_CH4/EVENTOUT
	PC10/SP3_SCK/I2S3_CK/UART4_TX/SDIO_D2/DCMI_D8/USART3_TX/EVENTOUT
	PC11/UART4_RX/SP3_MISO/SDIO_D3/DCMI_D4/USART3_RX/I2S3ext_SD/EVENTOUT
	PC12/UART5_TX/SDIO_CK/DCMI_D9/SP3_MOSI/I2S3_SD/USART3_CK/EVENTOUT
	PC13/EVENTOUT/RTC_AF1
	PC14-OSC32_IN/PC14/EVENTOUT/OSC32_IN
	PC15-OSC32_OUT/PC15/EVENTOUT/OSC32_OUT

STM32F427IH
2MB
256KB

Title		
<Title>		
Size	Document Number	Rev
A3	<Doc>	<Rev Code>
Date:	Friday, December 15, 2017	Sheet 3 of 11

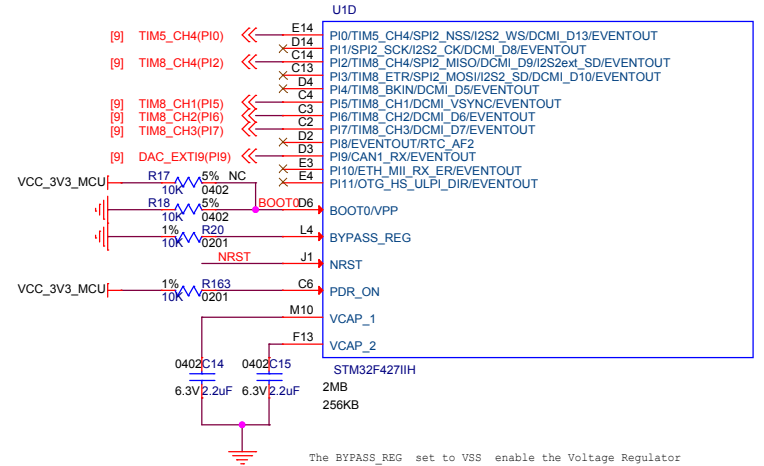
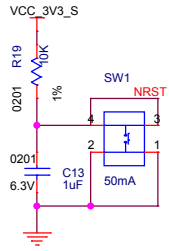
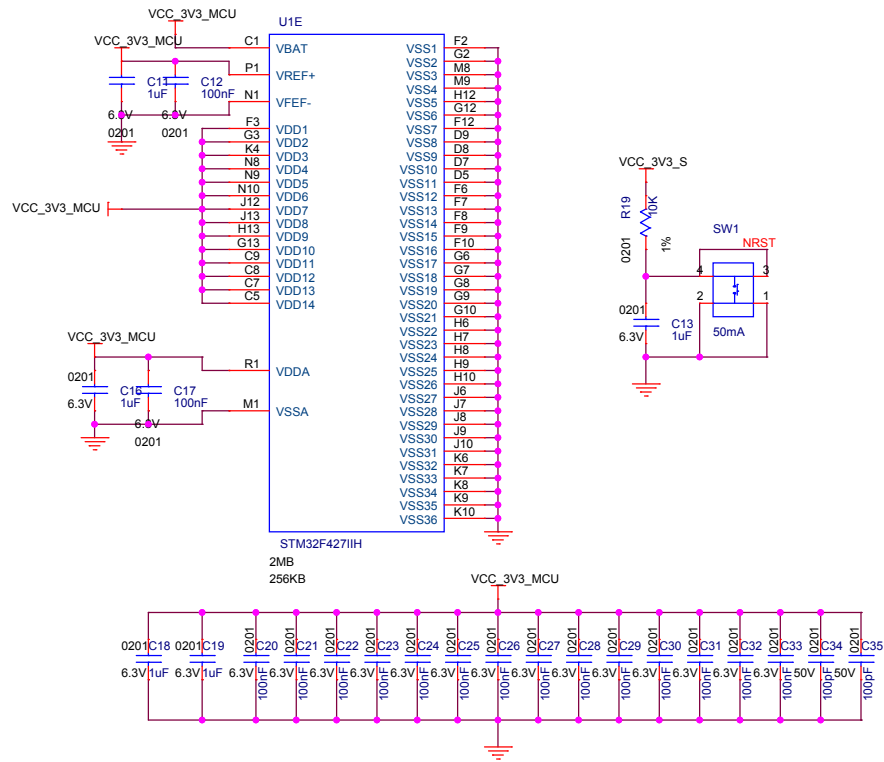
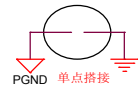
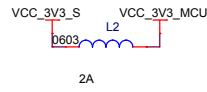


STM32F427IHH
2MB
256KB



STM32F427IHH
2MB
256KB

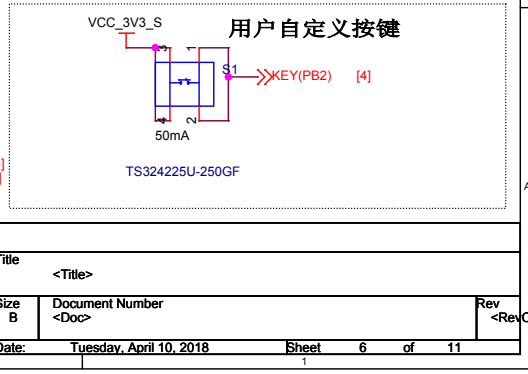
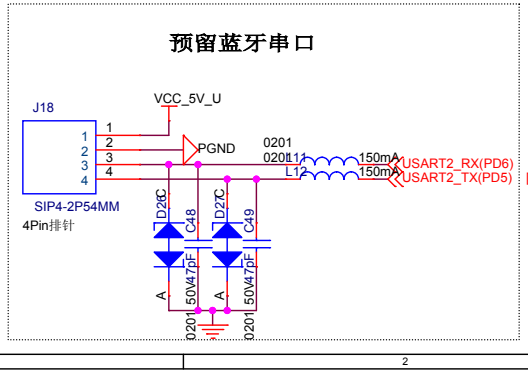
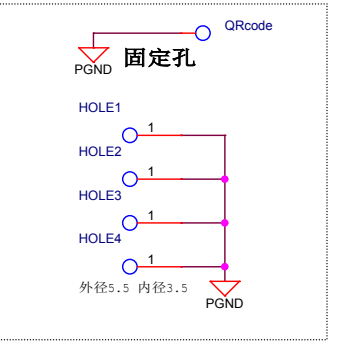
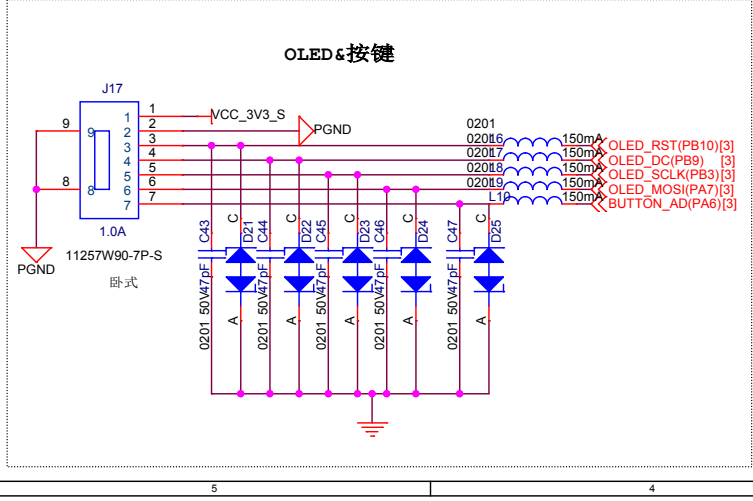
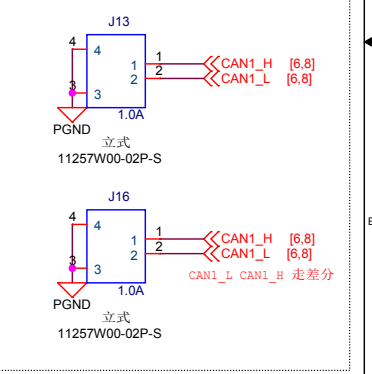
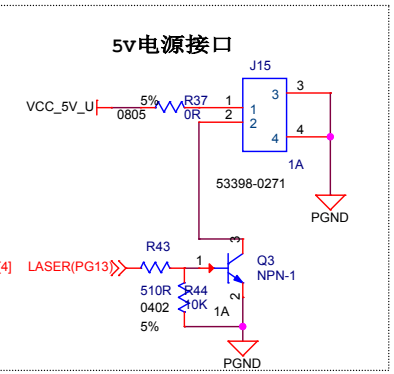
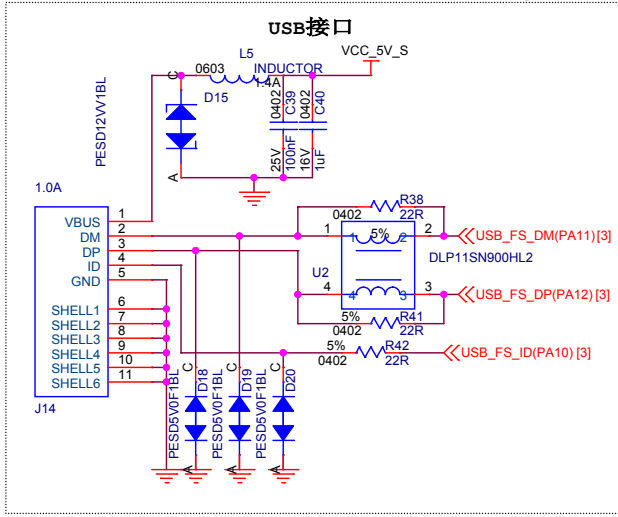
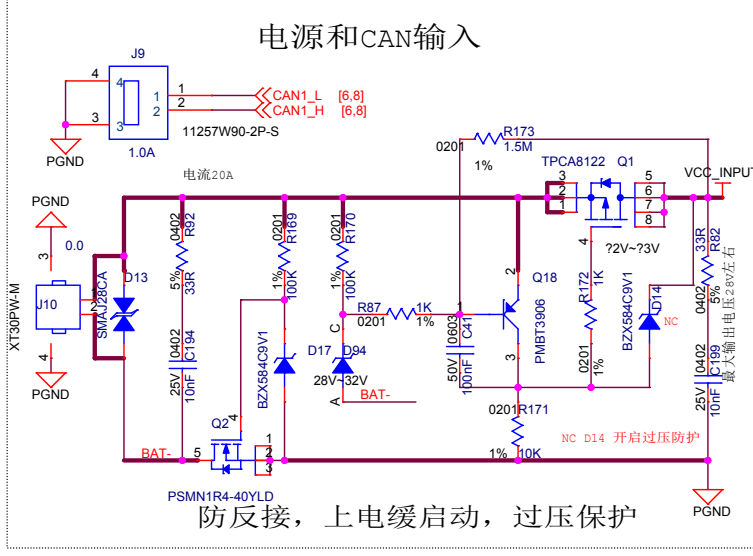
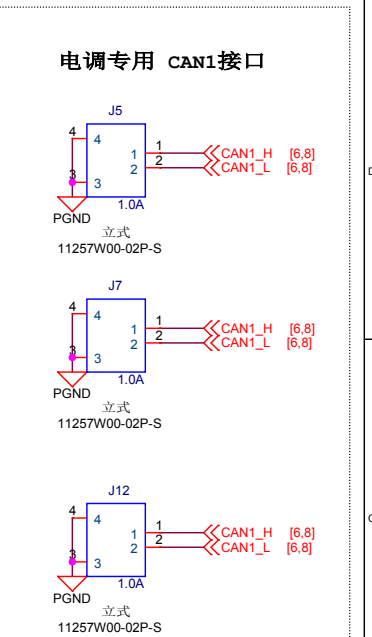
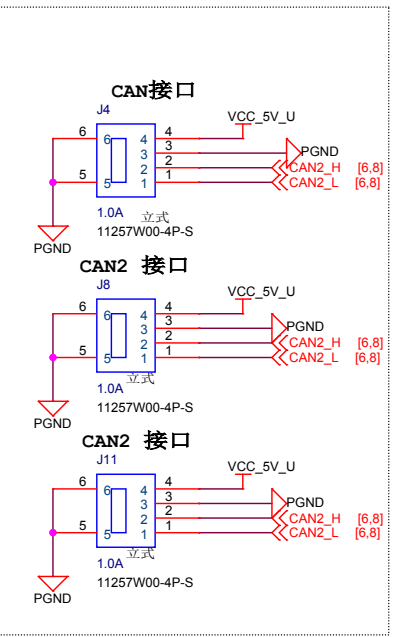
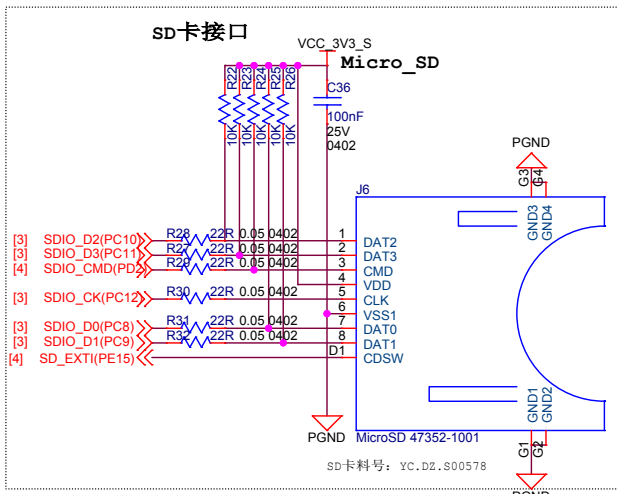
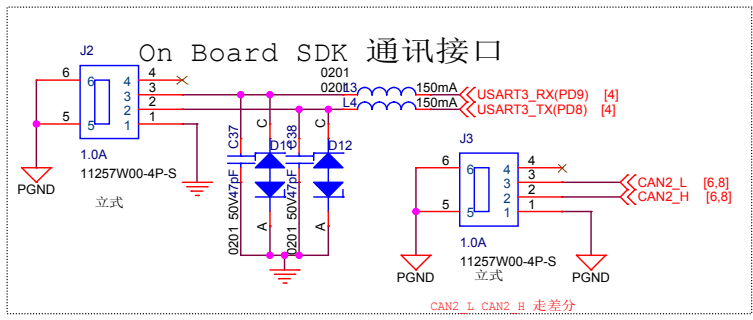
Title		<Title>
Size	Document Number	Rev
A3	<Doc>	<Rev>
Date:	Tuesday, April 10, 2018	Sheet 4 of 11



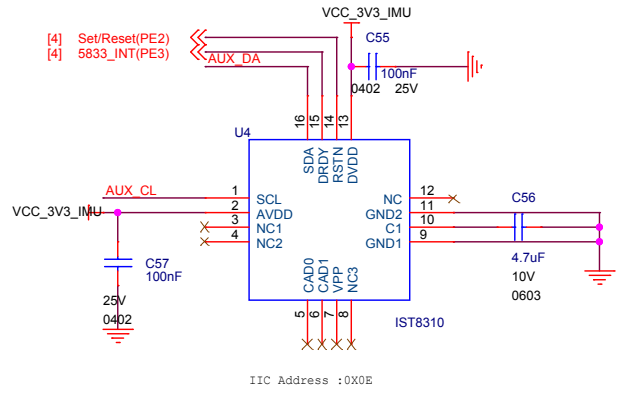
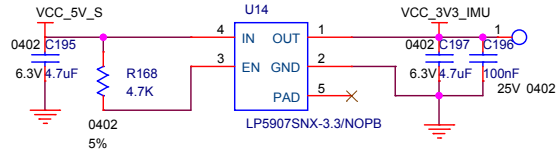
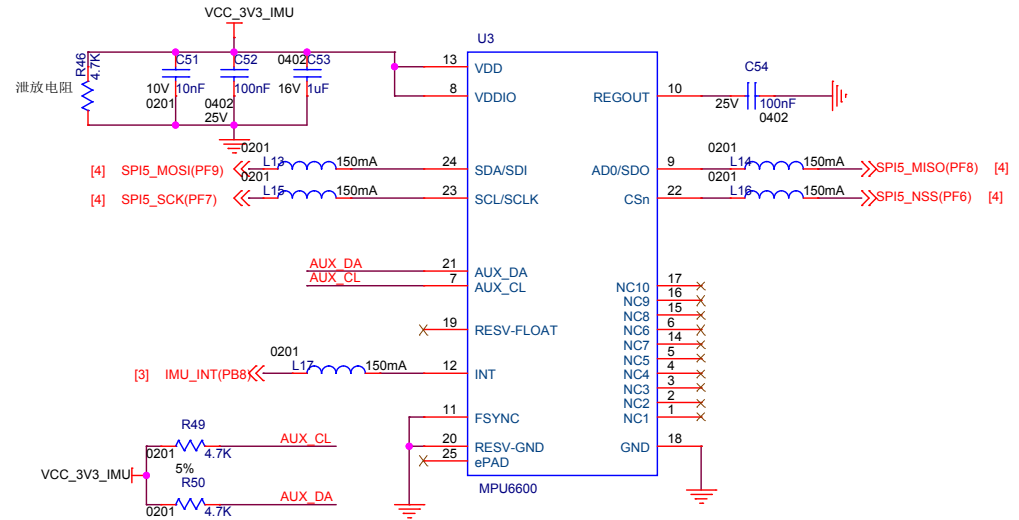
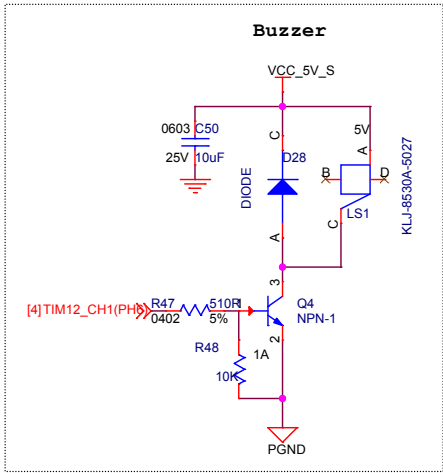
The BYPASS_REG set to VSS enable the Voltage Regulator
The Voltage regulator to optimize the power performance
If enable the Voltage, the VCAPx should be connected to 2.2µF capacitor to ground

BOOT1	BOOT0	BOOT SOURCE
X	0	User Flash
0	1	System Memory
1	1	Embedded SRAM

通过短接nc电阻来改变boot引导方式。



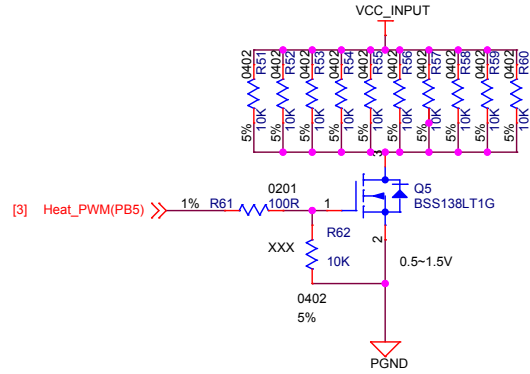
Title	<Title>	
Size	Document Number	Rev
B	<Doc>	<RevCode>
Date:	Tuesday, April 10, 2018	Sheet 6 of 11



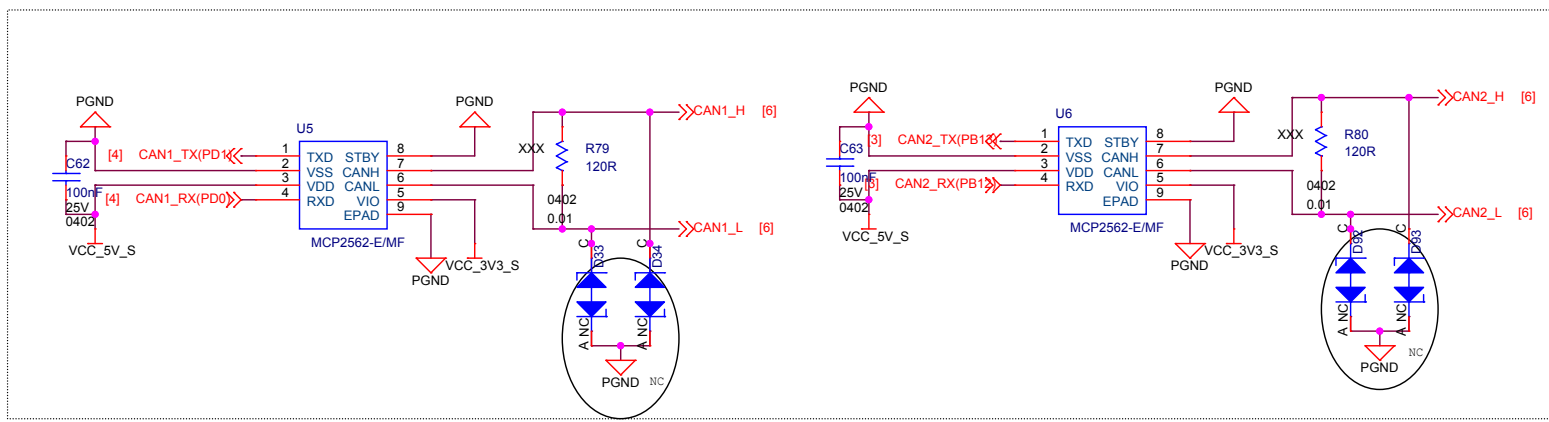
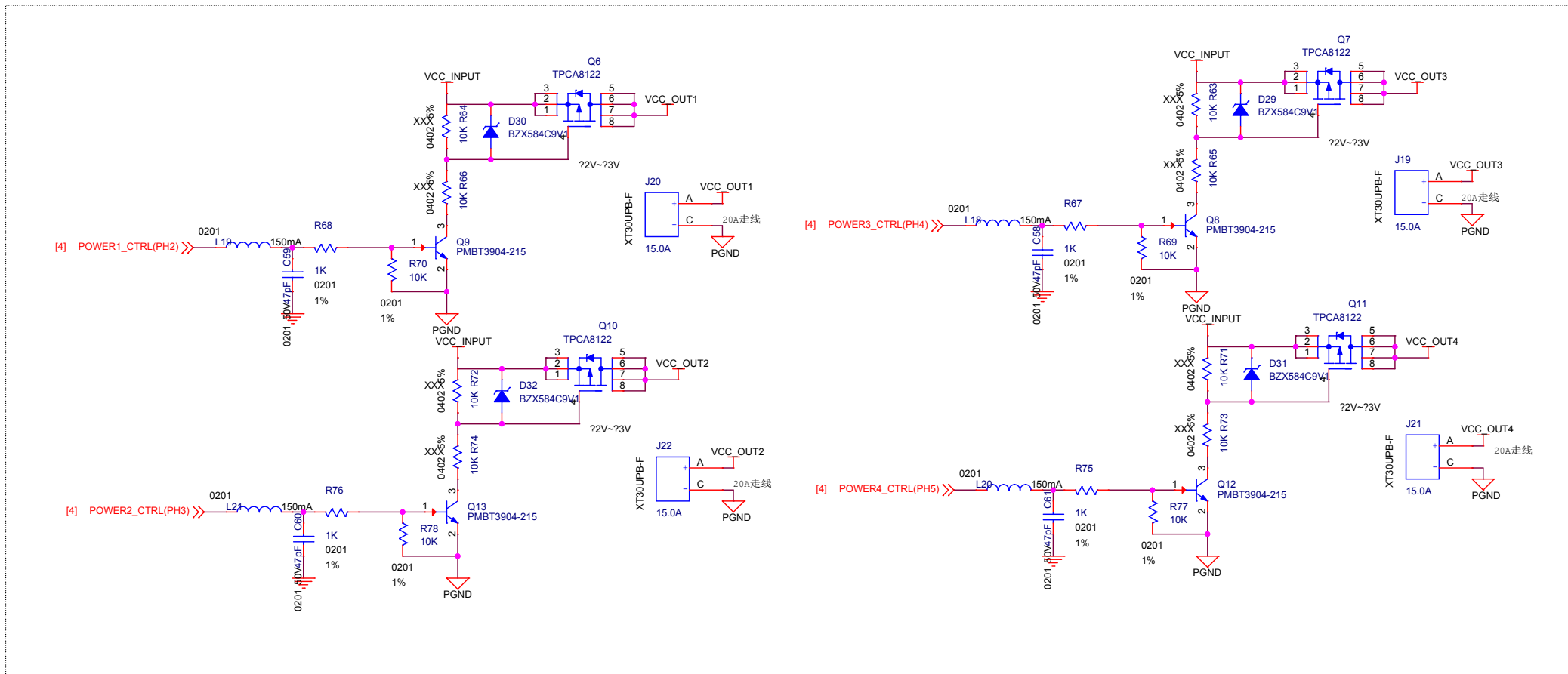
Slave Address Select

CAD1	CAD0	Address
VSS	VSS	0CH
VSS	VDD	0CH
VDD	VSS	0EH
VDD	VDD	0FH

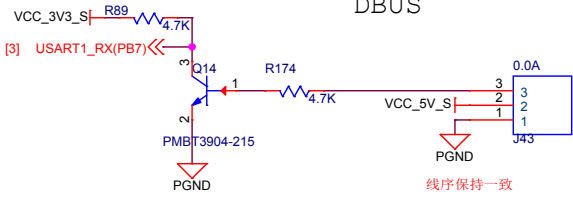
*if CAD1 and CAD0 are floating, I2C address will be 0EH



Title		<Title>
Size B	Document Number	Rev <RevCode>
Date:	Friday, January 05, 2018	Sheet 7 of 11



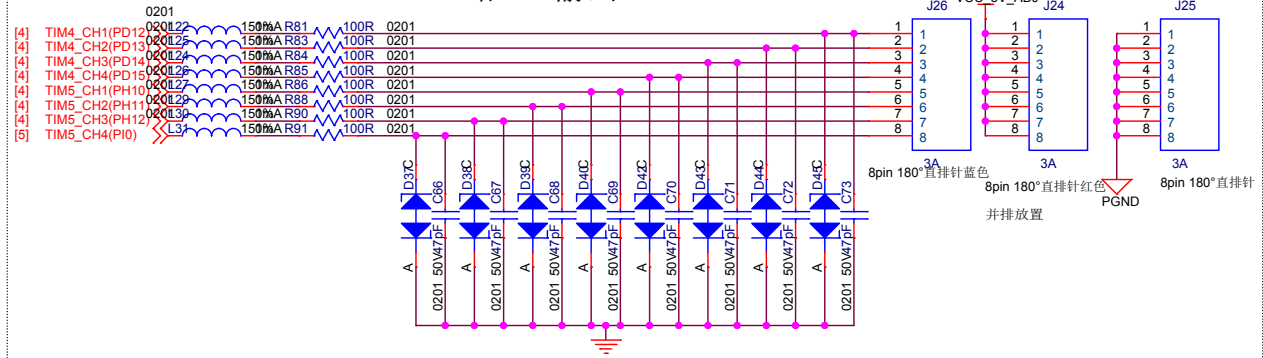
Title	<Title>	
Size	Document Number	Rev
B	<Doc>	<RevCode>
Date:	Tuesday, December 12, 2017	Sheet 8 of 11



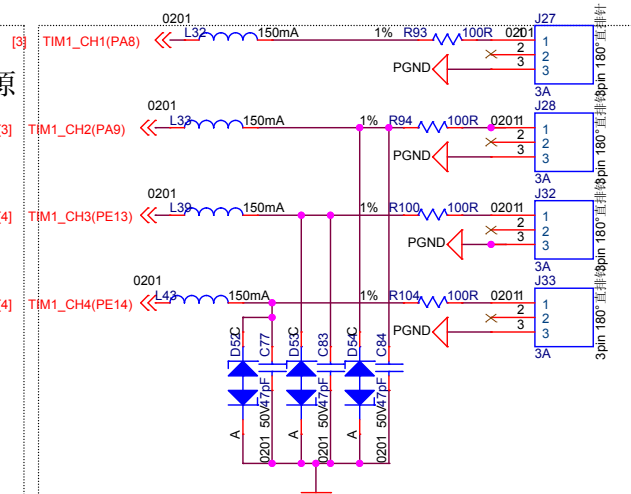
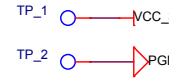
DBUS

线序保持一致

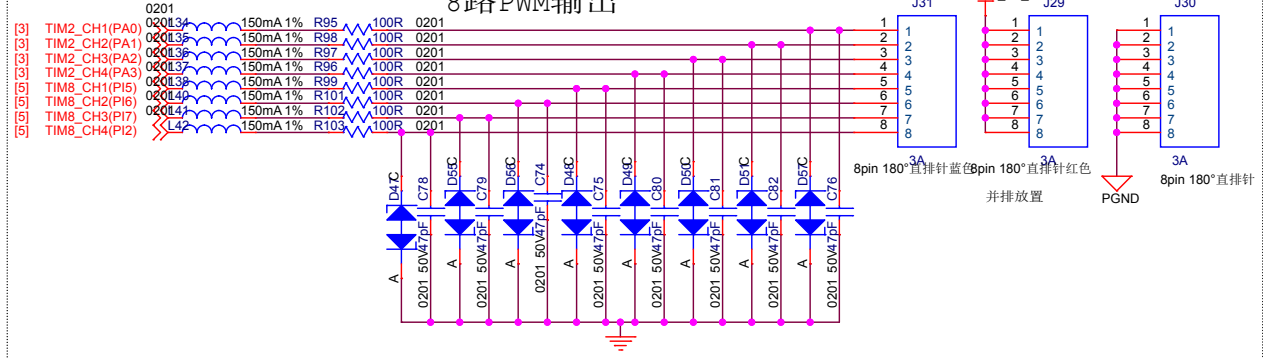
8路PWM输出



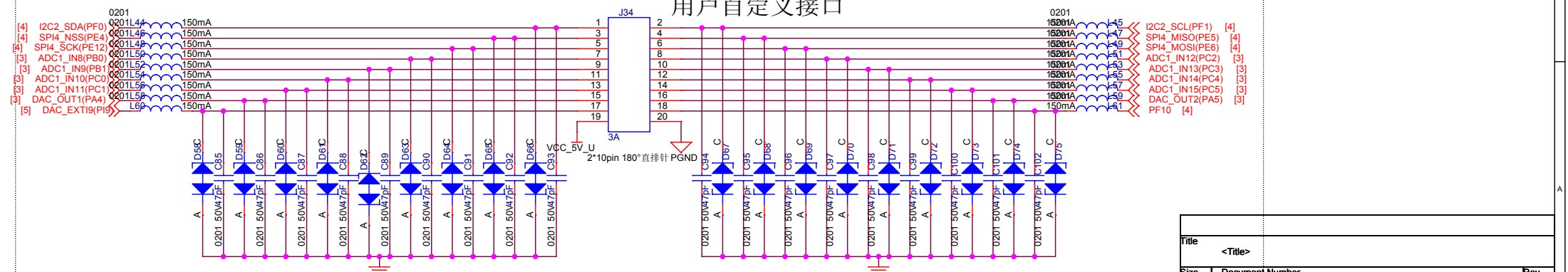
3V@3A用户电源



8路PWM输出

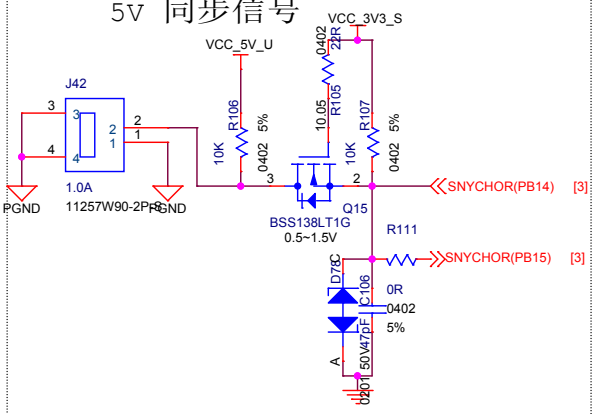


用户自定义接口

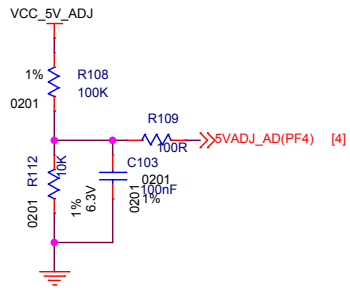


Title	<Title>	
Size	Document Number	Rev
B	<Doc>	<Rev/Code>
Date:	Tuesday, April 10, 2018	Sheet 9 of 11

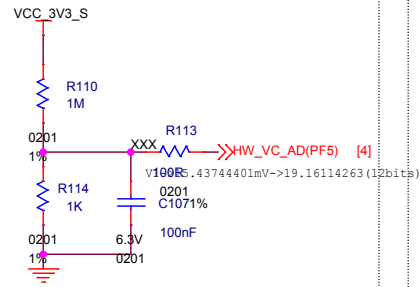
5V 同步信号



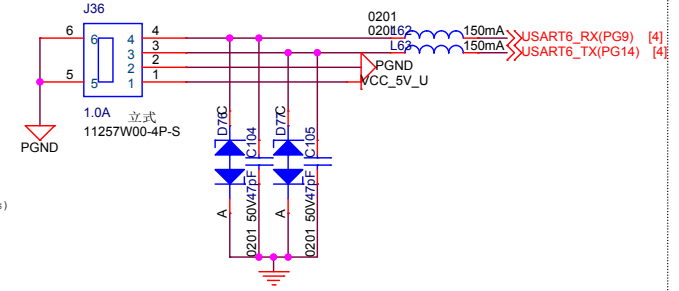
可调5V电源电压采集



硬件版本控制



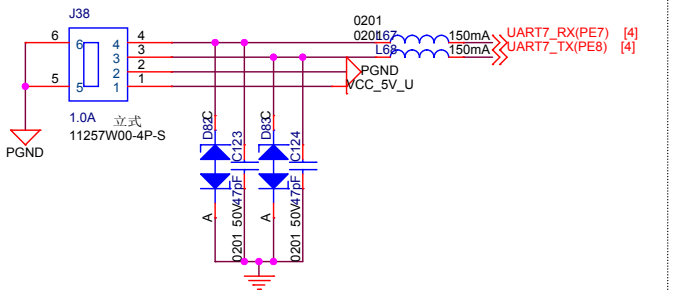
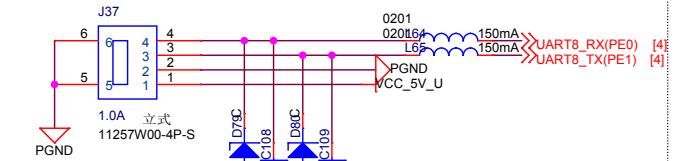
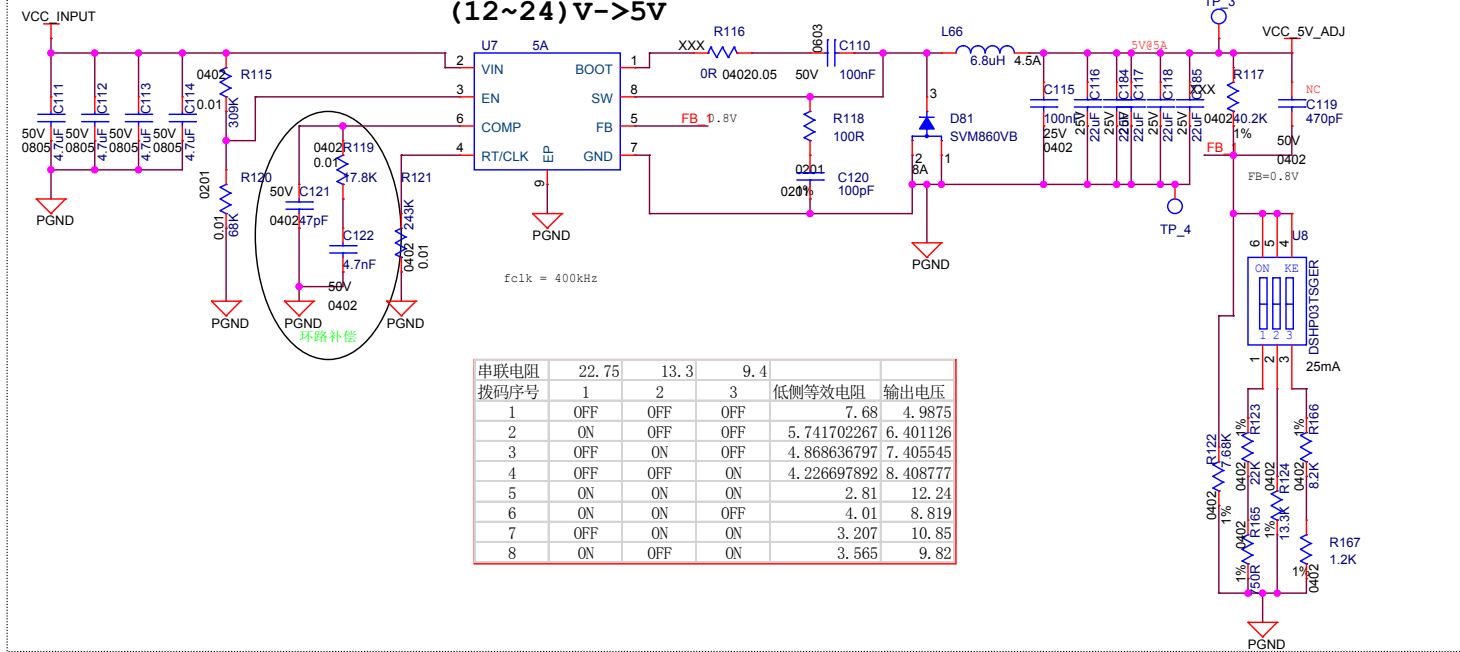
USER串口



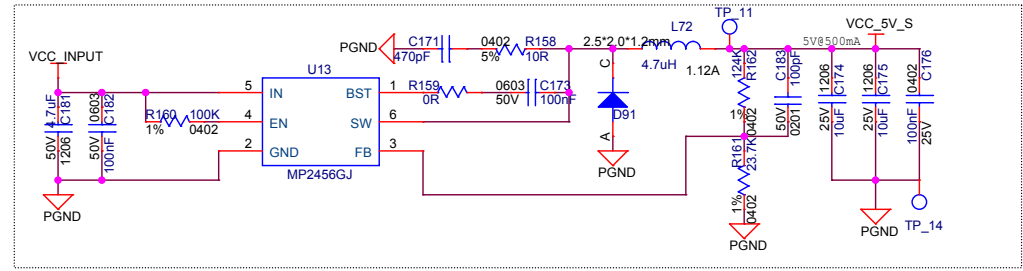
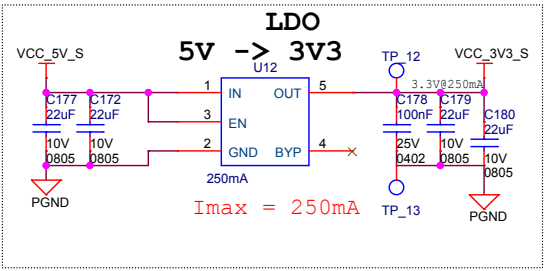
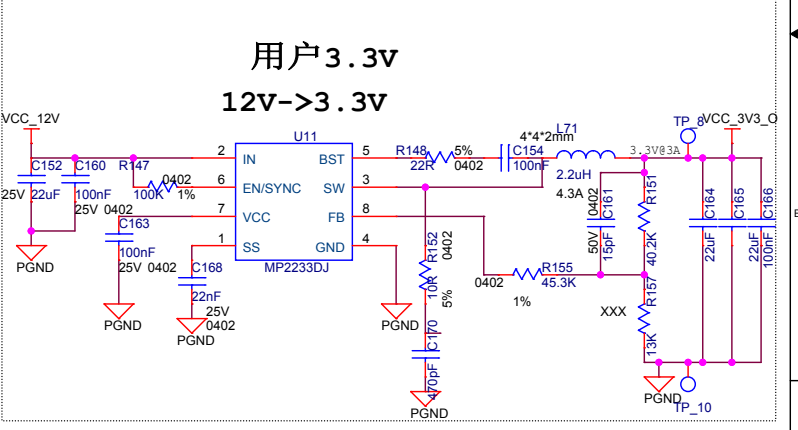
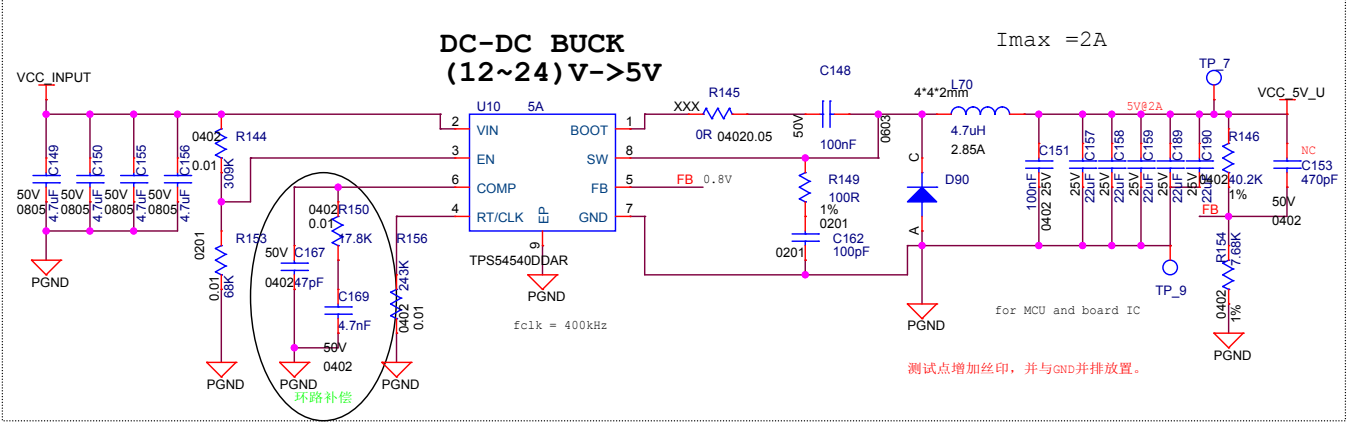
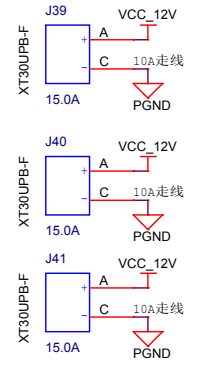
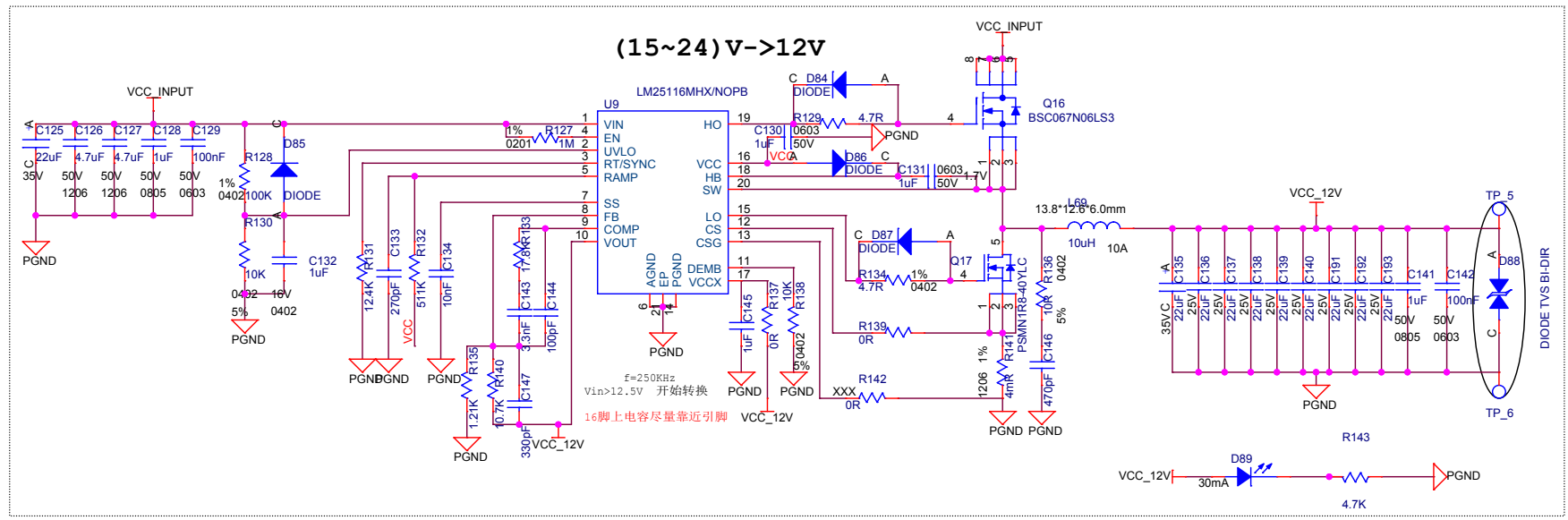
舵机四级可调电源

DC-DC BUCK (12~24)V->5V

Imax = 5A



Title		<Title>
Size	Document Number	Rev
B	<Doc>	<RevCode>
Date:	Tuesday, April 10, 2018	Sheet 10 of 11



Title	<Title>	
Size B	Document Number <Doc>	Rev <RevCode>
Date	Thursday, March 08, 2018	Sheet 11 of 11